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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,370	12/09/1999	LOUIS A. LIPPINCOTT	10559/105001	8772

20985 7590 10/22/2003

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EXAMINER	
HESSELTINE, RYAN J	

ART UNIT	PAPER NUMBER
2623	10

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/458,370	LIPPINCOTT, LOUIS A.	
	Examiner	Art Unit	
	Ryan J Hesseltine	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-17,19-21,23-26 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19-21,23-26 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *16 July 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 16, 2003 has been entered.

Drawings

2. The drawings were received on July 16, 2003. These drawings are acceptable.

Response to Arguments

3. Applicant's arguments filed July 16, 2003 have been fully considered but they are not persuasive. On page 9, third paragraph, applicant states, "Tanaka does show a sequencer block, but does not show that two different inverse discrete cosine transforming functions can be concurrently carried out into same directions." The examiner respectfully disagrees. Tanaka discloses a switching circuit 18 of the address generator that switches the row and column addresses. As an example, Tanaka discloses that the addresses are first designated in the row direction wherein the results calculated by the one-dimensional DCT calculator 4 are written to the memory device 2 in row direction (column 11, line 9-15). Tanaka goes on to describe how each memory location is read and transmitted to the one-dimensional DCT calculator 6 and subsequently the results from the one-dimensional DCT calculator 4 are written to the same address, then the memory address is incremented and the reading and writing operations are performed repeatedly until the last memory location is reached (column 11, line 16-40). This

section exemplifies Tanaka's process shown in Figure 9, in a control operation of the reading-writing control section 12, the data of a designated address are read and transmitted to the one-dimensional DCT calculator 6 at a low voltage level of a clock signal CK in one cycle, and the calculated results of the one-dimensional DCT calculator 4 are written to the same designated address fro the period of a high voltage level of the clock signal in this cycle (column 10, line 64-column 11, line 5). The examiner would also like to point out that, while most of the discussion in Tanaka is related to the discrete cosine transform (DCT), it is also disclosed that the construction of an inverse discrete cosine transform (IDCT) is similar (column 13, line 23-25).

Claim Objections

4. Claims 1, 15, and 23 objected to because of the following informalities:

- Line 5-6 of claim 1 states, "to operate on a matrix of coefficients in concurrently two same directions and to periodically..." This is confusing and would make more sense if reworded such as: "to concurrently operate on a matrix of coefficients in *the same* direction and..."
- Line 7-8 of claim 15 states, "executing a second one-dimensional discrete cosine transform..." It is believed applicant intended this to read, "executing a second one-dimensional *inverse* discrete cosine transform". Line 13 of claim 15 states, "the matrix of intermediate results". It is unclear which matrix of intermediate results is being used in this step since two intermediate matrices are created.
- Claim 22, listed on page 6 as "Original", was cancelled in the amendment filed March 11, 2003 and thus has not been addressed.

- Claim 23, listed on page 7 of the instant amendment has been amended but is incorrectly labeled as "Original" in line 1. In addition, line 7-8 states, "one of two states, each state indicating the direction of operation of both each one-dimensional inverse discrete cosine". The phrase "operation of both each one-dimensional..." is confusing; it would make more sense if reworded such as "operation of both one-dimensional..."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-17, 19-21, 23-26, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (USPN 5,268,853, previously cited), hereafter Tanaka.

7. Regarding claim 1, Tanaka discloses a method of implementing a two-dimensional inverse discrete cosine transform, comprising: executing two one-dimensional inverse discrete cosine transforming functions, each of the functions being controlled to operate on a matrix of coefficients (column 5, line 12-17) in concurrently two same directions (column 11, line 16-40; column 15, line 10-28).

8. Regarding claim 8, Tanka discloses a method capable of causing a machine to: execute two one-dimensional inverse discrete cosine transforming functions, each of the functions being controlled to operate on a matrix of coefficients in either of two (index U/V) different directions

(column 5, line 12-17) but carrying out both of said functions in the same direction concurrently, and periodically changing said direction (column 11, line 16-40; column 15, line 10-28).

9. Regarding claim 15, Tanaka discloses a method of implementing a two-dimensional inverse discrete cosine transform (column 5, line 12-17), comprising: first executing a first one-dimensional inverse discrete cosine transforming function in a first direction on a first matrix of coefficients to produce a matrix of intermediate results (column 11, line 9-15); second, after said first executing, executing a second one-dimensional [inverse] discrete cosine transform in a second, different direction on a second matrix of coefficients to produce another matrix of intermediate results; executing a third one-dimensional inverse discrete cosine transforming function in said second direction on the matrix of intermediate results concurrent with said second executing in the second direction on said second matrix of coefficients (column 11, line 16-40; column 11, line 58 to column 12, line 10), and periodically switching and executing between the first and second directions (column 11, line 16-20; column 15, line 10-28).

10. Regarding claim 19, Tanaka discloses a method capable of causing a machine to: execute a first one-dimensional inverse discrete cosine transforming function, where the first function executes in a first direction on a first matrix of coefficients, producing a matrix of intermediate results (column 11, line 9-15); and execute a second one-dimensional inverse discrete cosine transform on a second direction on a second matrix of coefficients; execute a second one-dimensional inverse discrete cosine transforming function, where the second function executes in said second direction on the matrix of intermediate results concurrent with execute a second function on the second matrix of coefficients (column 11, line 16-40; column 11, line 58 to

column 12, line 10), in which the functions switch periodically and concurrently between the first and second directions (column 11, line 16-20; column 15, line 10-28).

11. Regarding claims 23 and 25, Tanaka discloses an apparatus/computer implementing a two-dimensional inverse discrete cosine transform, comprising: two one-dimensional inverse discrete cosine transform blocks (figure 11, elements 4 and 6); a memory block (figure 11, elements 2a and 2b); a sequencer block (figure 6, element 18; figure 11, elements 20 and 22), the sequencer block alternately being in one of two states, each state indicating the direction of operation of both each one-dimensional inverse discrete cosine transform block (column 6, line 50-55; column 11, line 9-20); and an address generator block (figure 5, element 8; column 6, line 56-65).

12. Regarding claims 2, 9, 16, and 20, Tanaka discloses that one of the directions is row order (column 7, line 66-68).

13. Regarding claims 3, 10, 17, and 21, Tanaka discloses that one of the directions is column order (column 7, line 66-68).

14. Regarding claims 4 and 11, Tanaka discloses that a sequencer determines which direction each function operates in for a given matrix (figure 6, element 18; column 11, line 16-17).

15. Regarding claims 5 and 12, Tanaka discloses that an address generator generates an address for each coefficient in the matrix (column 5, line 55-59).

16. Regarding claims 6 and 13, Tanaka discloses that said executing executes the functions concurrently in the same direction on two different matrices of coefficients (column 11, line 16-40; column 12, line 4-10).

17. Regarding claims 7 and 14, Tanaka discloses that the functions are concurrently executed in the same direction (column 12, line 4-10), the functions switching periodically and concurrently to the other direction (column 11, line 16-40; column 15, line 10-28).

18. Regarding claims 24 and 26, Tanaka discloses that the address generator block is to generate addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer (column 11, line 16-40).

19. Regarding claim 28, Tanaka discloses that said second one-dimensional inverse discrete cosine transforming function and said third one-dimensional inverse discrete cosine transforming function occur concurrently in the same direction (column 11, line 16-40; column 15, line 10-28).

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- USPN 6,628,714 to Fimoff et al. discloses down converting MPEG encoded high definition sequences to lower resolution by applying a vertical or horizontal operator to first DCT coefficients to produce intermediate results, and apply concurrently to adjacent blocks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J Hesseltine whose telephone number is 703-306-4069. The examiner can normally be reached on Monday - Friday, 8:30 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on 703-308-6604. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

rjh
October 15, 2003